High Speed, Low Power ALU Design using Reversible Logic Gates based onVedic Mathematics

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Abstract-In today's era nanocomputing attracts more interest due to ability of processors to perform complex and challenging processes with higher speeds. Processors speed depends greatly on multiplier, due to this regard multiplier unit employ Vedic mathematics sutras in computation algorithms which will reduce the complexity, execution time, area etc. In proposed design there are two techniques for multiplication they are Urdhva triyakbhyam sutra and Nikhilam sutra. As Urdhva triyakbhyam sutra performs faster for small inputs and Nikhilam sutra for larger inputs. Here a control circuit which by itself selects the appropriate multiplication sutra based on inputs. Also reversible logic acquires extent attention due to their ability to reduce the power dissipation which is the main motto behind low power circuit designs.

Keywords: appropriate, nanocomputing, Nikhilam, reversible logic, sutra, Urdhva triyakbhyam, Vedic.

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1. INTRODUCTION-

The speed of processor mostly depends on multiplier operation. This increases the demand for high speed multipliers along with efficient area and avoiding extremes power consumption.For low power consumption reversible logic play vital role in low-power circuit design. An Irreversible circuit dissipates energy due to information loss. Landauer's principles state clearly that, there is a minimum possible amount of energy required to change one bit of information known as Landauer limit:

kTln2

Where, k → Boltzmann constant ($1.38x10^{-23}$J/K)

T → Temperature

ln2→ natural log of 2 (0.69315)

At room temperature (25°c or 298.15 K), the Landauer limit represents an energy of approximately 0.0178 eV or 2.85 zJ.

In 1973, C.H. Bennett proposed that kTln2 energy would not dissipate as system permits the reproduction of the inputs from perceive outputs. Reversible logic represents the operation of running the system both forward and backward. This means that, we can generate inputs from outputs and can stop and go back to any point in the computation history. The motivation behind reversible logic is that maintains a quantity of information by uncomputing bits which will help in rising energy efficiency. Fundamentally energy efficiency resulting speed of circuits such as nanocircuits, also to increase the portability of devices reversible computing required. To make device more portable, reversible computing will reduce circuit element size limits, so in today's nanocomputing era, the need of reversible computing cannot be ignored. Vedic mathematics provides simple approach to mathematical computations. Vedic mathematics was lost to the modern world over several thousand years. Fortunately, the renowned scholar Jagadguru Swami Bharati Krishna Teerthji Maharaja (1884-1960), discovered 16 sutras and 13 up-sutras in the parishistha of Atharva Veda. After continuous sadhana and handwork, he was able to decode them and get wide ranging mathematical principles and applications from them. He found that these sutras cover all aspects of mathematical science in depth. Any mathematics like Algebra, Geometry or Trigonometry can be solved with these sutras. Vedic mathematics is logical and consistent than modern mathematics. The list so compiled contains Sixteen Sutras and Thirteen Sub - Sutras as stated hereunder.

Sl. No	Sutras	Sub sutras or Corollaries
1.	Ekādhikena Pūrvena (also a corollary)	Ānurūpyena
2.	Nikhilam Navataścaramam Daśatah	Śisyate Śesamjnah
3.	Ūrdhva - tiryagbhyām	Ādyamādyenantyamantyena
4.	Parāvartya Yojayet	Kevalaih Saptakam Gunỹat
5.	Sūnyam Samyasamuccaye	Vestanam
6.	(Ānurūpye) Sūnyamanyat	Yāvadūnam Tāvadūnam
7.	Sankalana - vyavakalanābhyām	Yāvadūnam Tāvadūnīkrtya Vargañca Yojayet
8.	Purānāpurānābhyām	Antyayordasake˙pi
9.	Calanā kalanābhyām	Antyayoreva
10.	Yāvadūnam	Samuccayagunitah
11.	Vyastisamastih	Lopanasthāpanabhyām
12.	Śesānyankena Caramena	Vilokanam
13.	Sopantyadvayamantyam	Gunitasamuccayah Samuccayagunitah
14.	Ekanyūnena Pūrvena	
15.	Gunitasamuccayah	
16.	Gunakasamuccayah	

Fig:1 Vedic Mathematics Sutras

NIKHILAM NAVATASCARAMAM DASATAH

"Nikhilam Navatascaramam Dasatah", which literally translated means: all from 9 and the last from 10".
Suppose we have to multiply 9 by 7.

1. We should take, as base for our calculations that power of 10 which is nearest to the numbers to be multiplied. In this case 10 itself is that power. (10) 9 – 1 7 – 3 6 / 3

2. Put the numbers 9 and 7 above and below on the left hand side (as shown in the working alongside here on the right hand side margin);

3. Subtract each of them from the base (10) and write down the remainders (1 and 3) on the right hand side with a connecting minus sign (–) between them, to show that the numbers to be multiplied are both of them less than 10.

4. The product will have two parts, one on the left side and one on the right. A vertical dividing line may be drawn for the purpose of demarcation of the two parts.

5. Now, the left hand side digit can be arrived at in one of the 4 ways a) Subtract the base 10 from the sum of the given numbers (9 and 7 i.e. 16). And put (16 – 10) i.e. 6 as the left hand part of the answer 9 + 7 – 10 = 6 or b) Subtract the sum of two deficiencies (1 + 3 = 4) from the base (10) you get the same answer (6) again 10 – 1 – 3 = 6 or c) Cross subtract deficiency 3 on the second row from the original number 9 in the first row. And you find that you have got (9 – 3) i.e. 6 again 9 – 3 = 6 or d) Cross subtract in the converse way (i.e. 1 from 7), and you get 6 again as the left hand side portion of the required answer 7 – 1 = 6.

6. Now vertically multiply the two deficit figures (1 and 3). The product is 3. And this is the right hand side portion of the answer (10) 9 – 1

7. Thus 9 × 7 = 63. 7 – 3 6 / 3 This method holds good in all cases and is therefore capable of infinite application.

URDHVA TIRYAGBHYAM

Urdhva Tiryagbhyam sutra which is the General Formula applicable to all cases of multiplication and will also be found very useful later on in the division of a large number by another large number. The formula itself is very short and terse, consisting of only one compound word and means "vertically and cross-wise." The applications of this brief and terse sutra are manifold.

A simple example will suffice to clarify the modus operandi thereof. Suppose we have to multiply 12 by 13.

(i) We multiply the left hand most digit 1 of the multiplicand vertically by the left hand most digit 1 of the multiplier get their product 1 and set down as the left hand most part of the answer;

(ii) (ii) We then multiply 1 and 3 and 1 and 2 crosswise add the two get 5 as the sum and set it down as the middle part of the answer; and 12 13
1:(3 + 2):6 ➔156

(iii) We multiply 2 and 3 vertically get 6 as their product and put it down as the last the right hand most part of the answer. Thus 12 × 13 =156. Thus an efficient ALU which has high speed, low power and consume little bit wide area proposed to design using reversible gates based on Vedic Mathematics.

2. LITERATURE REVIEW-

Irreversibility and heat generation during computation was shown in [1]. The amount of heat dissipated for every irreversible bit operation is given by kTln2. He also showed that only the logically irreversible steps in a computation carry an unavoidable energy penalty. If we go with reversible operation, there would be no lower limit on energy consumption. Logical reversibility of computation by

C.H. Bennett highlighted in [2], kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way. He presented his idea with the help of Turing machine, ideal model of a computer that reads, writes and erases symbols on a tape, where machine note down about erased or overwritten data. At the end of computation, the final answer can be copied onto yet another tape for safekeeping. Then the machine is put in reverse gear and with the help of the history tape, all the operations are undone until the system returns to its initial condition. Efficient Building Blocks for Reversible Sequential Circuit Design in [3].They proposed the design of new reversible logic gate which is more suitable for designing multivalued reversible logic. In this paper they proposed the reversible flip-flops and latch using Fredkin gate, Toffli gate and Feynman gate. These designs are highly effective for reducing garbage outputs.Efficient design of Reversible Sequential Circuit in [4] they proposed 'Mamun' gate for the optimized reversible D Latch and JK Latch. Digital multiplier with reversible logic in [5]which was based on the formulas of the Ancient Indian Vedic Mathematics.Also the proposed multiplier design used for cryptographic purposes in the secure communication field. Implementation of multiplier using Kcm and Vedic mathematics by using reversible adder in [6] proposed for higher performance of higher order bit multiplication multiplier, i.e. for 16X16 and more, the multiplier get realized by lower order bit multipliers like 8X8. In [7] they reported that a novel complex number multiplier design based on the Vedic mathematics sutras effective for high speed complex arithmetic circuits. In this they, shown advantages of Vedic mathematics in encounters the stages and reduction in partial products.

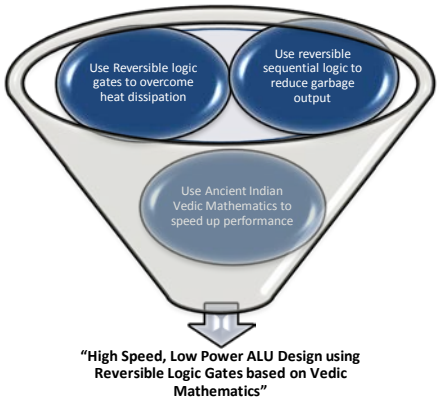

Fig:2

CONCLUSION-

We have presented an approach to design high speed processor which will withstand for nanocomputing technologies by using Vedic algorithms. Along with speed, the requirement of power is reduced as we design with reversible logic gates.

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